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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,559	10/09/2001	Nai-Shung Chang	JCLA5775	7171

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J C PATENTS, INC.
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EXAMINER	
YANCHUS III, PAUL B	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 11/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/974,559	CHANG, NAI-SHUNG	
	Examiner	Art Unit	
	Paul B Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 8-10* is/are rejected.

7)☒ Claim(s) *4-7 and 11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

Claims 4-7 and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner et al., US Patent no. 6,269,443 [Poisner], in view of, AMD Duron Processor Data Sheet [AMD].

Regarding claim 1, Poisner discloses a system capable of automatically reading-out a multiple value of clock frequency from system bus, comprising:

a central processing unit [processor] having a storage unit therein [clock frequency multiplier register], wherein said storage unit holds a multiple value of clock frequency [column 4, lines 20-25]; and

a chipset [System Logic Device in Figure 2], wherein said chipset is capable of repeatedly selecting a multiple value of clock frequency until a synchronizing multiple clock frequency is found [column 3, line 42 – column 4, line 7 and column 4, lines 10-25].

Poisner discloses a system capable of automatically reading-out a multiple value of clock frequency and adjusting a processor clock speed multiplier accordingly, but does not explicitly disclose utilizing a serial initialization packet (SIP) protocol for communication between the processor and the chipset. AMD discloses that SIP is a well known protocol that is used to communicate configuration information from a chipset to a processor [pages 34 and 35]. It would have been obvious to one of ordinary skill in the art to use the well known SIP protocol for communication between the processor and the chipset in the Poisner system to ensure compatibility with conventional computer components.

Regarding claims 2 and 3, Poisner discloses that the chipset tries to implement the fastest possible clock frequency multiplier at first and then tries successively smaller multipliers until the processor is able to operate normally [column 4, lines 10-17]. Poisner does not explicitly state that a counter is used to generate the successively smaller multipliers in the system. However, Poisner inherently discloses a counter since some sort of counting means would have to be used in order to produce the successively smaller multiplier values.

Regarding claim 8, Poisner discloses a method of automatically reading-out a multiple value of clock frequency between a central processing unit and a system bus, wherein said central processing unit provides said multiple value of clock frequency, comprising said steps of:

selecting a multiple value of clock frequency [column 4, lines 20-30]; and

attempting to synchronize with said central processing unit by varying said preset multiple value of clock frequency [column 4, lines 20-30].

Poisner discloses a method of automatically reading-out a multiple value of clock frequency and adjusting a processor clock speed multiplier accordingly, but does not explicitly disclose utilizing a serial initialization packet (SIP) protocol for communication between the processor and the chipset. AMD discloses that SIP is a well known protocol that is used to communicate configuration information from a chipset to a processor [pages 34 and 35]. It would have been obvious to one of ordinary skill in the art to use the well known SIP protocol for communication between the processor and the chipset in the Poisner method to ensure compatibility with conventional computer components.

Regarding claims 9 and 10, Poisner discloses that the chipset tries to implement the fastest possible clock frequency multiplier at first and then tries successively smaller multipliers until the processor is able to operate normally [column 4, lines 10-17]. Poisner does not explicitly state that a counter is used to generate the successively smaller multipliers in the system. However, Poisner inherently discloses a counter since some sort of counting means would have to be used in order to produce the successively smaller multiplier values.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

He, US Patent no. 5,862,351, discloses automatically adjusting the clock frequency multiplier of a processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
November 15, 2004

JOHN R. COTTINGHAM
PRIMARY EXAMINER